IN THE CLAIMS:

Please cancel claims 1-21 without prejudice or disclaimer and add the following new claims:

1-21. (canceled).

22. (new) A method, comprising:

identifying a race condition in a circuit;

generating a netlist model for the circuit;

providing a virtual delay element in the netlist model;

providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit; and

generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element.

A4

23. (new) The method as recited in claim 22, further comprising:

selectively providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.

24. (new) The method of claim 22, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.

25. (new) The method of claim 24, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.

26. (new) The method of claim 25, wherein the physical characteristic comprises a delay characteristic.

27. (new) The method of claim 26, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.

28. (new) A system, comprising:

a processor; and

a memory coupled to the processor, the memory storing a program adapted to:

identify a race condition in a circuit;

generate a netlist model for the circuit;

provide a virtual delay element in the netlist model;

provide a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit; and

generate a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element.

29. (new) The system as recited in claim 28, wherein the program is further adapted to selectively provide a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.

30. (new) The system of claim 28, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.

31. (new) The system of claim 30, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.

32. (new) The system of claim 31, wherein the physical characteristic comprises a delay characteristic.

33. (new) The system of claim 32, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.

34. (new) A set of instructions residing in a storage medium, the set of instructions being capable of execution by a processor to implement a method, the method comprising:

identifying a race condition in a circuit;

generating a netlist model for the circuit;

providing a virtual delay element in the netlist model;

providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit; and

generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element.

35. (new) The set of instructions as recited in claim 34, wherein the method further comprises:

selectively providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.

36. (new) The set of instructions of claim 34, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.

37. (new) The set of instructions of claim 36, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.

38. (new) The set of instructions of claim 37, wherein the physical characteristic comprises a delay characteristic.

39. (new) The set of instructions of claim 38, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.